

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-161705

(43)Date of publication of application : 23.06.1995

(51)Int. Cl.

H01L 21/316

H01L 21/768

(21)Application number : 05-304196

(71)Applicant : NEC CORP

(22)Date of filing : 03.12.1993

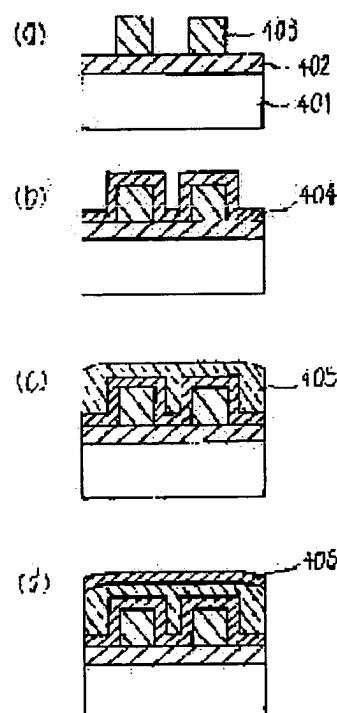
(72)Inventor : HONMA TETSUYA
MURAO YUKINOBU

(54) METHOD OF FORMING INTERLAYER INSULATING FILM OF MULTILAYERED WIRING OF SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To form an interlayer insulating film of multilayered wiring which generates no cavities in fine wiring gaps, has an excellent flatness, contains little residual water, and shows a low hygroscopicity, by forming a silicon oxide film containing fluorine by a specific method, after a first insulating film whose main component is silicon oxide is formed.

CONSTITUTION: A lower layer wiring 403 is formed on a semiconductor substrate 401 via an insulating film 402, and a first insulating film 404 whose main component is silicon oxide is formed on the whole surface containing the lower layer wiring 403. A silicon oxide film 405 containing fluorine groups is formed by chemical vapor deposition method using fluoroalkoxysilane having 3 or more C alkyl group [chemical formula: $\text{FnSi(OR)}_4\text{-n}$, n: 1,2,3, R: 3 or more C alkyl group] and oxidizing gas. A second insulating film 406 whose main component is silicon oxide is formed. For example, at least one out of water vapor, ozone, oxygen and oxygen denitride is used as the oxidizing gas.



LEGAL STATUS

[Date of request for examination] 24.06.1994

[Date of sending the examiner's decision of rejection] 16.12.1997

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2000 Japan Patent Office

*** NOTICES ***

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] Especially this invention relates to the formation method of the layer insulation film of the multilayer-interconnection structure about the manufacture method of a semiconductor device.

[0002]

[Description of the Prior Art] There is the method of depositing a silicon oxide as the formation method of the conventional layer insulation film for multilayer interconnections by using hetero alkoxysilane [the alkyl group of general formula : $\text{Si}(\text{OR})\text{n}4(\text{OR}')\text{-n}$, $\text{n}:1, 2$ and 3R , and the R' : carbon numbers 1-3] as a raw material (JP,2-153072,A). This 1st conventional silicon-oxide deposition puts this into an evaporator, keeps the solution temperature at 42 degrees C, using dimethoxy diethoxysilane [chemical formula: $\text{Si}(\text{OCH}_3)_2 2 (\text{OC two H}_5)$] as a raw material, and is N_2 as carrier gas. N_2 which passed to the evaporator by the flow rate of 3 l/min., and included the dimethoxy JIEKI lion run The distributed machine of a reaction chamber is supplied. Simultaneously, it is O_2 to an ozonizer. It passes by the flow rate of 7.5 l/min., and is O_3 with an ozonizer. O_3 made into the concentration of 9500 ppm N_2 which supplied the gas distribution machine of the quality of a reaction, and contained the above-mentioned dimethoxy diethoxysilane It mixes in a gas distribution machine and a reactor is supplied by the pressure of 760Torr. A silicon oxide is deposited for the temperature of the silicon wafer put on the susceptor in a reaction chamber as 400 degrees C or 300 degrees C.

[0003] Moreover, BUIERU id eye in 1991 Multi-level Interconnection conference As it is in P.435 of proceedings (1991 Multilevel Interconnection Conference Proceedings), there is the method of forming a silicon oxide at constant temperature (150 degrees C or less) more using a steam and a tetraethyl orthochromatic silicate [$\text{Si} (\text{OC two H}_5)_4$]. The plasma-chemistry vapor growth is used for this 2nd conventional technology, and by impressing RF power intermittently, it forms a fluid high silicon oxide and performs flattening of a layer insulation film. The schematic diagram of the plasma-chemistry vapor-growth equipment used for drawing 8 with this conventional technology is shown. This equipment is used and it is 30sccm, 120sccm, and N_2 used as carrier gas of the flow rate of a tetraethyl orthochromatic silicate and $\text{H}_2 \text{ O}$, respectively. A flow rate is controlled to 400sccm(s) and the silicon oxide is formed on an aluminum circuit pattern on the conditions which become pressure 10Torr and the substrate temperature of 120 degrees C. Here, in RF power (frequency of 13.56MHz), it is referred to as 300W and is impressing intermittently, and it is the conditions which duty [-time /(ON time +OFF time) x100%] becomes 30 to 50%, a fluidity increases, and flat nature improves.

[0004]

[Problem(s) to be Solved by the Invention] The Prior art mentioned above had the following problems. That is, in the 1st conventional technology, from membrane formation temperature being as high as 300-400 degrees C, the tensile stress which remains is large, and after forming a silicon oxide by this method on aluminum wiring, defects, such as a void, occur in aluminum wiring, and there is a problem that wiring resistance is increased or disconnected. Moreover, since it does not have a fluidity and the irregularity on the front face of a substrate is reflected as it is, the silicon oxide formed on the substrate which has a wiring level difference by this method has the problem that a cavity occurs in the fault or the detailed wiring gap that surface flattening is difficult. Furthermore, moisture tends to remain, and the silicon oxide formed by this method has the fault that hygroscopicity is high, and also has the problem of degrading a device property. Therefore, it is difficult for the 1st conventional technology to present practical use.

[0005] Moreover, there are the following problems with the 2nd conventional technology. That is, from performing film formation at low temperature 150 degrees C or less, since moisture and the organic substance remain so much and this remains moisture and organic substance are emitted in a next heat treatment process into the formed silicon oxide, a silicon oxide contracts, there is a fault that a crack will go into a silicon oxide, as a result, and there is a problem that thick-film-izing is difficult. Furthermore, it has the fatal fault that remains moisture will degrade a device property, like the 1st conventional technology. Therefore, it is difficult to present practical use also with the 2nd conventional technology.

[0006] the purpose of this invention canceled the trouble of the conventional technology mentioned above, i.e., it is to excel in flat nature and offer [a cavity does not occur in a detailed wiring gap, but] the formation method of a multilayer-interconnection layer insulation film with few remains moisture contents and the amounts of moisture absorption again

[0007]

[Means for Solving the Problem] The formation method of the multilayer-interconnection layer insulation film of the 1st

semiconductor device of this invention The process which forms lower layer wiring through an insulator layer on a semiconductor substrate, and the process which forms the 1st insulator layer which makes a silicon oxide a principal component all over including this lower layer wiring top, By the chemical-vapor-deposition method using the fluoro alkoxysilane [the (OR)_{4-n}, n:1, 2 and 3, and three or more R:carbon numbers alkyl group] and the oxidizing gas which have a three or more-carbon number alkyl group [chemical formula :FnSi] It has the process which forms a fluorine content silicon oxide, and the process which forms the 2nd insulator layer which makes a silicon oxide a principal component continuously.

[0008] The formation method of the multilayer-interconnection layer insulation film of the 2nd semiconductor device of this invention The process which forms lower layer wiring through an insulator layer on a semiconductor substrate, and the process which forms the 1st insulator layer which makes a silicon oxide a principal component all over including this lower layer wiring top, In the chemical-vapor-deposition method using the fluoro alkoxysilane [Chemical formula :FnSi (OR')_{4-n}, and n = carbon numbers [1, 2, 3 and one or more R':carbon numbers] alkyl group] and the oxidizing gas which have an one or more-carbon number alkyl group When the boiling point makes the steam of a high boiler 90 degrees C or more add, it has the process which forms a fluorine content silicon oxide, and the process which forms the 2nd insulator layer which makes a silicon oxide a principal component continuously.

[0009] Moreover, it sets by the chemical-vapor-deposition method of the 1st of this invention, and the formation method of the 2nd semiconductor device multilayer-interconnection layer insulation film. Tetrapod alkoxysilane [Chemical formula : Si (OR")₄ and R":alkyl group], Alkyl alkoxysilane (chemical formula :R"_n Si(OR")_{4-n} you may add at least one of alkyl group), an organic siloxane, and organic silanes to n, n:1, 2 and 3, and R"R" 'independence.)

[0010] Furthermore, in the 1st of this invention, and the formation method of the multilayer-interconnection layer insulation film of the 2nd semiconductor device, after forming a fluorine content silicon oxide, you may use together the flattening process which uses at least one of the etchback method, the grinding method, and the applying methods.

[0011] In the chemical-vapor-deposition method an insulator layer is furthermore formed on a front face including wiring by this invention This insulator layer adds and forms a halogenation inorganic substance in an organic silane ozone system, The silicon-oxide film by the above-mentioned organic silane ozone system ordinary-pressure CVD It forms on the 1st silicon-oxide film currently formed by the organic silane system plasma CVD method on the wiring which prepared alternatively (it is hereafter called a new oxide film) on the semiconductor substrate. The process which carries out etchback of all of the aforementioned organic silica films, and the front face of the above-mentioned new oxide film by reactive ion etching, and carries out flattening after carrying out the spin application of the organic silica film on the above-mentioned new oxide film, The process which forms the 3rd silicon-oxide film by the organic silane plasma CVD method on the above-mentioned new oxide film is included.

[0012] Moreover, after forming on the wiring which prepared the new oxide film of the above-mentioned publication alternatively on the semiconductor substrate and carrying out the spin application of the organic silica film on the above-mentioned new oxide film, etchback of all of the aforementioned organic silica films and the front face of the above-mentioned new oxide film is carried out by reactive ion etching, and the process which carries out flattening, and the process which forms the 2nd silicon-oxide film by the organic silane plasma CVD method on the above-mentioned new oxide film are included.

[0013] In the chemical-vapor-deposition method an insulator layer is furthermore formed on a front face including wiring by this invention This insulator layer adds a halogenation organic silane in an organic silane ozone system in the shape of a pulse, and is formed in it, The silicon-oxide film by the above-mentioned organic silane ozone system ordinary-pressure CVD It forms on the 1st silicon-oxide film currently formed by the organic silane system plasma CVD method on the wiring which prepared alternatively (it is hereafter called a halogen pulse addition oxide film) on the semiconductor substrate. The process which carries out etchback of all of the aforementioned organic silica films, and the front face of the above-mentioned halogen pulse addition oxide film by reactive ion etching, and carries out flattening after carrying out the spin application of the organic silica film on the above-mentioned halogen pulse addition oxide film, The process which forms the 3rd silicon-oxide film by the organic silane plasma CVD method on the above-mentioned halogen pulse addition oxide film is included.

[0014] Moreover, the halogen pulse addition oxide film of the above-mentioned publication is formed on the wiring alternatively formed on the semiconductor substrate. The process which carries out etchback of all of the aforementioned organic silica films, and the front face of the above-mentioned halogen pulse addition oxide film by reactive ion etching, and carries out flattening after carrying out the spin application of the organic silica film on the above-mentioned halogen pulse addition oxide film, The process which forms the 2nd silicon-oxide film by the organic silane plasma CVD method on the above-mentioned silicon-oxide film is included.

[0015]

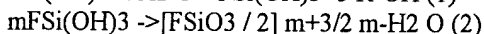
[Example] Next, this invention is explained with reference to a drawing.

[0016] Drawing 1 is the schematic diagram of the chemical-vapor-deposition equipment used for multilayer-interconnection layer insulation film formation of the semiconductor device which are the 1st of this invention, and the 2nd example. It sets to this drawing and is O2. A flow rate is controlled by the flow controller 106, and gas is introduced into an ozonator 105, and ozone is generated and it introduces into a reaction chamber from the dispersion head 104. It is N2 simultaneously. Gas is controlled by the flow controller 108,109,110,111 and it introduces into PABURA 112,113,114,115, and after making tetraethyl orthochromatic sill KETO [Si (OC two H5)₄] maintained at respectively fixed temperature, FUTSUORO alkoxysilane [FnSi(OR)_{4-n}, n:1, 2 and 3, and R:alkyl group], pure water, and a high boiler evaporate, it introduces into a reaction chamber from the dispersion head 104. It is mixed in a reaction chamber and these gas is formed on the semiconductor substrate 101 on

the susceptor 103 maintained at fixed temperature at the heater 102 for heating. About the chemical-vapor-deposition method using fluoro alkoxysilane and pure water, Japanese Patent Application No. 3-006312, Japanese Patent Application No. 3-136426, and Japanese Patent Application No. 4-095117 have described how to use fluoro triethoxysilane.

[0017] In the 1st example, membranes were formed using fluoro alkoxysilane and pure water. The temperature of BAPURA of fluoro alkoxysilane and pure water is kept at 40 degrees C, respectively, and it is N₂ for bubbling. The flow rate was set to 1SLM and 4SLM, respectively. Moreover, N₂ The flow rate of carrier gas was set to 3SLM(s), and reaction chamber internal pressure was set to about 760 Torr(s). Moreover, substrate temperature was made into 25 degrees C. As fluoro alkoxysilane Fluoro trimethoxysilane [FSi (O) [OCH₃] Four kinds of 3] and fluoro triethoxysilane [FSi (OC two H₅)₃] fluoro trinor mull propoxysilane [FSi (n-OC three H₇)₃] and a fluoro triisopropoxy silane [FSi (i-OC three H₇)₃] are used. The fluorine content silicon oxide with a thickness of about 0.5mm was formed on the semiconductor substrate which has an aluminum-Si-Cu circuit pattern with a thickness of about 1 micrometer. angle theta d to the level surface of the FUTSU system content silicon-oxide side attachment wall in about 1 micrometer in thickness when drawing 2 changes the alkyl group of fluoro trialkoxysilane, and the space portion of the aluminum-Si-Cu circuit pattern of 0.8 micrometers of ****, angle theta m to the level surface of an aluminum-Si-Cu wiring side attachment wall, and its ratio -- theta d/theta m is shown Flow nature is so high that this angle ratio is large, and excelling in embedded nature is shown. When the thing using the normal propoxy group, i.e., fluoro trinor mull propoxysilane, [FSi (n-OC three H₇)₃] is used among four kinds of fluoro trialkoxysilane from this drawing, an angle ratio is the largest and is about 1.02. When fluoro trinor mull propoxysilane is used, high flow nature is obtained, and this shows that laying under the ground of a wiring space is performed good. This flow nature can be explained as follows. That is, of the reaction of fluoro trialkoxysilane [FSi (OR)₃ and R:alkyl group] and a steam, as shown in a formula (1) and (2), respectively, a fluorine or fluoro alkoxysilane itself serves as a catalyst, a adding-water decomposition reaction and a condensation polymerization reaction occur, and a FUTSU system content silicon oxide is formed.

[0018]



(m : positive integer) Here, R-OH, i.e., alcohol, occurs as a reaction by-product by the formula (1). SiO₂ by which this alcohol was generated by the reaction It adheres to a substrate front face in the state where it stuck to intermediate field [FSiO 3/2] m, and a fluorine content silicon oxide is formed of surface reaction. Here, it will be SiO₂ if this alcohol cannot evaporate easily (i.e., if vapor pressure is small). Intermediate field tend to flow, and what stuck to the wiring upper part is considered to flow between wiring spaces, therefore it is thought that flow nature is high and laying-under-the-ground nature increases.

[0019] It is thought that the alcohol generated when fluoro trimethoxysilane, fluoro triethoxysilane, fluoro trinor mull propoxysilane, and a fluoro triisopropoxy silane are used is methyl alcohol, ethyl alcohol, normal propyl alcohol, and isopropyl alcohol, respectively, in 25 degrees C (membrane formation temperature), such vapor pressure is 125Torr(s), 58Torr, 20Torr, and 44Torr, respectively, and its vapor pressure of normal propyl alcohol is the smallest in this. This is in agreement with angle ratio theta d/theta m becoming large most, when fluoro trinor mull propoxysilane is used.

[0020] Furthermore, when the FUTSU system content silicon oxide with a thickness of about 1 micrometer was formed on the semiconductor substrate which has an aluminum-Si-Cu circuit pattern similarly, in the pattern whose space between wiring is 0.4 micrometers, generating of a cavity was not seen at all between wiring spaces only within the case where fluoro trinor mull propoxysilane is used.

[0021] Moreover, a FUTSU system content silicon oxide with a thickness of about 0.4 micrometers is similarly formed on a P type silicon substrate, and the result which measured the infrared absorption spectrum (FFIR spectrum) is shown in drawing 3. In this drawing, the infrared absorption spectrum of the silicon oxide formed at the temperature of 350 degrees C under the ordinary pressure is shown, using a tetraethyl orthochromatic silicate (TEOS) and ozone as comparison. In this drawing, although the big absorption peak which originates in OH basis wave number abbreviation 3400cm⁻¹ is looked at by the infrared absorption spectrum (this drawing (e)) of the silicon oxide using TEOS and ozone, it turns out that most absorption peaks resulting from OH basis are not seen at the infrared absorption spectrum of the fluorine content silicon oxide formed using four fluoro trialkoxysilane shown in this drawing (a) - (d). It is shown that the fluorine content silicon oxide which formed this, using fluoro trialkoxysilane and pure water as the gas source does not almost have remains moisture. Furthermore, compared with the amount (about 2%) of moisture absorption of the silicon oxide in which all the formed things for which the amount of moisture absorption calculated from the increase in a weight when keeping the formed FUTSU system content silicon oxide for 30 days in pure water used four kinds of fluoro trialkoxysilane are about 0.3 - 0.5%, and formed this using TEOS and ozone, it was 1/4 or less. Moreover, the threshold change of potential when forming a fluorine content silicon oxide on n type MOS transistor, impressing the voltage of 6V and 2V to a drain and a gate electrode, respectively, and performing the stress examination of 2 hours was about 2%, and was a sufficiently small value compared with the threshold change of potential (about 10%) of n type MOS transistor which has the silicon oxide formed using TEOS and ozone.

[0022] Next, the one section of the layer insulation film of aluminum wiring was formed on these conditions, using the high fluoro trinor mull propoxysilane and high pure water of flow nature as the gas source.

[0023] Drawing 4 is the process cross section showing the formation method of the multilayer-interconnection layer insulation film of the semiconductor device of this invention. As shown in drawing 4 (a), after forming the 1st silicon oxide 404 with a thickness of about 0.4 micrometers by the plasma-chemistry vapor growth on the aluminum wiring layer 403 with a thickness of about 1 micrometer formed on the semiconductor substrate 401 through the insulator layer (SiO₂ film) 402 with a thickness of

about 0.8 micrometers, The fluorine content silicon oxide 405 with a thickness of about 0.8 micrometers is formed at the temperature of 25 degrees C, using fluoro trinor mull propoxysilane [$\text{FSi}(\text{n-OC three H7})_3$] and pure water as the gas source. Next, the 2nd silicon oxide 406 with a thickness of about 0.4 micrometers is again formed by the plasma-chemistry vapor growth. According to the above process, the high layer insulation film of flat nature has been formed. In the pattern whose space between aluminum wiring is 0.4 micrometers, there is not no generating of a cavity and the crack was not generated at all on a layer insulation film.

[0024] Next, in order to make flat nature improve further, the grinding method was used together and the flattening layer insulation film was formed. The process cross section is shown in drawing 5. As shown in drawing 5 (a), (b), and (c), on the semiconductor substrate 501 After forming the insulator layer (SiO_2 film) 502 with a thickness of about 0.8 micrometers, the aluminum wiring layer 503 with a thickness of about 1 micrometer, the 1st plasma-chemistry vapor-growth silicon oxide 504 with a thickness of about 0.4 micrometers, and the fluorine content silicon oxide 505 with a thickness of about 2 micrometers one by one, as shown in this drawing (d) It grinds until the thickness of the fluorine content silicon oxide 505 on wiring is set to about 0.4 micrometers. In polish of a fluorine content silicon oxide, it is SiO_2 . The conditions which become about 30 psis about the rotation speed of about 100 rotations and a load per minute in the polish pad of polyurethane nature were used pouring the alkaline-water solution of an impalpable powder continuously. Then, as shown in this drawing (e), the 2nd silicon oxide 506 with a thickness of about 0.5 micrometers is formed by the plasma-chemistry vapor growth. The layer insulation film formed at the above process does not have the dependency of the thickness by the circuit pattern, and the completely flat front face was obtained. Moreover, it was what crack initiation does not have in a layer insulation film.

[0025] Although this example described the case where fluoro trialkoxysilane and pure water were used as the gas source, the same effect is acquired even if it adds at least one of tetrapod alkoxysilane, such as a tetraethyl ARUSO silicate (TEOS), alkyl alkoxysilane, an organic siloxane, and organic silanes to these.

[0026] Furthermore, although pure water is used as the oxidizing gas source, the same effect is acquired even if this uses ozone, ozone, pure water and ozone, oxygen and ozone, 2 nitriding oxygen, pure water, oxygen and pure water, and 2 nitriding oxygen. Membrane formation temperature has good 150 degrees C or less at best still more preferably below 300 degrees C. In this example, the number of the formation conditions of a fluorine content silicon oxide is one, and it is possible especially to change a quantity of gas flow etc. suitably.

[0027] Furthermore, by this example, although aluminum is used as a wiring material, even if this uses at least 1 of contest polysilicon, metal silicide, an aluminium alloy, a titanium alloy, a tungsten alloy, gold, copper, and platinum, or the wiring which consists of these laminated structures, the same effect is acquired.

[0028] Next, the 2nd example of this invention is explained with reference to a drawing. this example describes how to add a high boiler steam at the time of the fluorine content silicon-oxide formation which uses fluoro trialkoxysilane and pure water.

[0029] In the membrane formation equipment shown in drawing 1, a bubbler 113 and a bubbler 115 are filled up with fluoro triethoxysilane [$\text{FSi}(\text{OC two H5})_3$] and normal propyl alcohol [$\text{n-C three H7 and OH}$], respectively, bubbler temperature is fixed to 40 degrees C, respectively, and it is the object N_2 for bubbling. The quantity of gas flow was fixed to 1SLM, respectively. The temperature of the bubbler 114 with which pure water was furthermore filled up is kept at 40 degrees C, and it is the object N_2 for bubbling. The quantity of gas flow was set to 4SLM(s). Other conditions formed membranes on an example 1 and these conditions. The fluorine content silicon oxide with a thickness of about 0.5 micrometers was formed on the semiconductor substrate which has an aluminum-Si-Cu circuit pattern as well as an example 1. When fluoro trinor mull propoxysilane was used by making normal propyl alcohol add at the time of membrane formation although the ethoxy basis was used as an alkyl group in this example as shown in drawing 2, near angle ratio θ/θ_m (about 1.01) was obtained. This shows that it has an effect equivalent to the time of using fluoro trinor mull propoxysilane by adding a normal propyl alcohol steam in the chemical-vapor-deposition method for using fluoro triethoxysilane and pure water as the gas source.

[0030] A fluorine content silicon oxide with a thickness of about 0.4 micrometers is formed on a P type silicon substrate on these conditions at drawing 6, and the result which measured the infrared absorption spectrum (FT-IR spectrum) is shown. The size of the absorption peak (about 3400cm^{-1}) which the same spectrum as the time of fluoro trinor mull propoxysilane being used for the infrared absorption spectrum of the fluorine content silicon oxide formed using fluoro triethoxysilane and normal propyl alcohol is acquired from this drawing, and originates in OH basis shows that it is almost equivalent and there are few remains OH bases.

[0031] Furthermore, like the example 1, when flattening of the layer insulation film of aluminum wiring was performed, it was what generating of a cavity does not have and crack initiation does not have in a layer insulation film in a pattern with a wiring space interval of 0.4 micrometers like an example 1.

[0032] Although fluoro triethoxysilane is used as fluoro alkoxysilane in this example, this is good at at least one of a fluoro methoxy silane, a fluoroethoxy silane, fluoro propoxysilane, and fluoro butoxysilane. Moreover, as a high boiler, although normal propyl alcohol (boiling point of 97.4 degrees C) is used, the boiling point of this should just be a solvent 90 degrees C or more.

[0033] Moreover, although this example described the case where fluoro trialkoxysilane, pure water, and the three gas sources of a high boiler were used, the same result is obtained even if it adds at least one of tetrapod alkoxysilane, such as a tetraethyl orthochromatic silicate (TEOS), alkyl alkoxysilane, an organic siloxane, and organic silanes to these.

[0034] Furthermore, although pure water is used as the oxidizing gas source, the same effect is acquired even if ozone, ozone, pure water and ozone, oxygen and ozone, 2 nitriding oxygen, pure water, oxygen and pure water, and 2 nitriding oxygen are used for this. Membrane formation temperature has at best still more preferably good 150 degrees C or less below 300 degrees C. In

this example, the number of the formation conditions of a fluorine content silicon oxide is one, and it is possible especially to change a quantity of gas flow etc. suitably.

[0035] Furthermore, in this example, although aluminum is used as a wiring material, even if at least 1 of contest polysilicon, metal silicide, an aluminium alloy, a titanium alloy, a tungsten alloy, gold, copper, and platinum or the wiring which consists of these laminated structures is used for this, the same effect is acquired.

[0036] Next, the 3rd example of this invention is explained with reference to a drawing. Drawing 7 is the schematic diagram of the membrane formation equipment for the fluorine content silicon-oxide formation by the plasma-chemistry vapor growth which are the 3rd of this invention, and the 4th example. It is exhausted so that a reaction chamber 701 may become a constant pressure in this drawing, and a flow controller 708 is minded, and it is an ozonator 707O2. Gas is introduced and it is ozone / O2. Mixed gas is supplied in a reaction chamber. Moreover, the bubbler 714,715,716,717 is filled up with a tetraethyl orthochromatic silicate (TEOS), fluoro alkoxysilane, pure water, and the high boiler, respectively. Such gas source material is N2 controlled by the flow controller 710,711,712,713, respectively. Gas can perform bubbling. The RF power which has the frequency of 13 or 56MHz is supplied to the cathode electrode 703 in a reaction chamber. Moreover, it can become irregular by the pulse generator 706, and this RF power can supply the RF power on a pulse to the cathode electrode 703.

[0037] Moreover, the anode electrode 702 is grounded and the semiconductor substrate 705 is maintained at constant temperature by the heater 704 for heating. The fluorine content silicon oxide was formed in this example, using fluoro trinor mull propoxysilane [FSi (n-OC three H7)3], and an ETORA ethyl orthochromatic silicate [TEOS, Si (OC two H5)4] and pure water as the gas source. The bubbler of fluoro trinor mull propoxysilane, a tetraethyl orthochromatic silicate, and pure water is fixed to 40 degrees C, 40 degrees C, and 35 degrees C, respectively, and it is the object N2 for bubbling. The quantity of gas flow was set to 100sccm(s), 100sccm, and 300sccm, respectively, it introduced in the reaction chamber, and reaction chamber internal pressure was fixed to 10Torr(s). RF power was set to 300W and impressed continuously. Moreover, substrate temperature was made into 100 degrees C. When the fluorine content silicon oxide with a thickness of about 0.5 micrometers was formed using these conditions on the semiconductor substrate which has an aluminum-Si-Cu circuit pattern with a thickness of about 1 micrometer, in the pattern with a wiring space interval of 0.4 micrometers, good flow nature was obtained like the example 1. Furthermore, when the fluorine content silicon oxide with a thickness of about 1 micrometer was formed, the cavity was not generated at all in the space section of a pattern with a wiring space interval of 0.4 micrometers. When this example also formed the layer insulation film at the same process as an example 1, good flat nature was obtained similarly, and there was no cavity in the space section between wiring, and it was what is not crack ***** at the layer insulation film. Moreover, since a condensation polymerization reaction was promoted by the catalysis of a fluorine, there were few remains OH bases and they have formed the more precise fluorine content silicon oxide by the collision to the substrate front face of the active species in the inside of plasma.

[0038] In this example, although fluoro alkoxysilane and fluoro trinor mull propoxysilane are used, at least one of a fluoro methoxy silane, a fluoroethoxy silane, fluoro propoxysilane, and fluoro butoxysilane can be used for this by lowering growth temperature. Moreover, in this example, although pure water is used as a source material of a oxidizing gas, at least one of pure water, oxygen, ozone, and 2 nitriding oxygen can be used for this. Moreover, as an addition of a tetraethyl orthochromatic silicate, the range of 5 - 95 volume % is desirable. In this example, although the tetraethyl orthochromatic silicate (TEOS) is added, even if it does not add TEOS, the same effect is acquired. It is also possible to add a high boiler further again, and flow nature increases more. Moreover, membrane formation temperature is good below 250 degrees C, and its 100 degrees C or less are good preferably.

[0039] Next, the 4th example of this invention is explained with reference to a drawing. In this example, using fluoro trinor mull propoxysilane [FSi (n-OC three H7)3], and a tetraethyl orthochromatic silicate [TEOS, Si (OC two H5)4] and ozone as the gas source, as fluoro alkoxysilane, RF power was intermittently impressed the fixed period using the plasma-chemistry vapor-growth equipment shown in drawing 7, and the fluorine content silicon oxide was formed. It is the object N2 for bubbling, filling up a bubbler 715,714 with fluoro trinor mull propoxysilane and a tetraethyl orthochromatic silicate, respectively, and using each temperature as 40 degrees C. The quantity of gas flow was fixed to 100sccm(s) by the flow controller 711,710, respectively, and source gas was introduced in the reaction chamber. Simultaneously, it is O2. By the flow controller 708, the flow rate was controlled for gas to 500sccm(s), and it introduced into the ozonator 707, and the ozone of about 2 volume % was generated and it introduced in the reaction chamber. Reaction chamber internal pressure was set to about 15 Torr(s). RF power was set to 300W and RF power was intermittently impressed by the pulse generator 706. Here, ON of a pulse and OFF time were set to TON=6msec and TOFF=9msec, respectively, and duty [TON/(TON+TOFF) x100%] was made into 40%. Moreover, substrate temperature was made into 100 degrees C. When the fluorine content silicon oxide with a thickness of about 0.5 micrometers was formed on the semiconductor substrate which has an aluminum-Si-Cu circuit pattern with a thickness of about 1 micrometer using these conditions, in the pattern with a wiring space interval of 0.4 micrometers, still better flow nature was obtained rather than the example 3. This is SiO2 by applying RF power intermittently. It thinks because the flow time on the front face of a substrate of intermediate field becomes long. Furthermore, when the fluorine content silicon oxide with a thickness of about 1 micrometer was similarly formed on the semiconductor substrate which has an aluminum-Si-Cu circuit pattern, it was what generating of a cavity does not have in the space section of a pattern with a wiring space interval of 0.4 micrometers.

[0040] When the layer insulation film was formed at the process which shows this method to drawing 4 and 5 like an example 1, it was what good flat nature is obtained similarly, and a cavity does not have in the space section between wiring, and a crack does not have in a layer insulation film. Moreover, like the example 3, there were few remains OH bases and they have formed the precise fluorine content silicon oxide.

[0041] Also in this example, like an example 3, although fluoro trinor mull propoxysilane is used as fluoro alkoxysilane, at least one of a fluoro methoxy silane, a fluoroethoxy silane, fluoro propoxysilane, and fluoro butoxysilane can be used for this by lowering growth temperature. Moreover, as a oxidizing gas, although the mixed gas of ozone/oxygen is used, pure water, oxygen, 2 nitriding oxygen, and such mixture can be used as a gas source material besides this. Moreover, as an addition of a tetraethyl orthochromatic silicate, the range of 5 - 95 volume % is desirable. In this example, although the tetraethyl orthochromatic silicate is added, even if it does not add this, the same effect is acquired. Furthermore, the same effect is acquired even if it adds alkoxysilane other than a tetraethyl orthochromatic silicate, alkyl alkoxysilane, an organic siloxane, and an organic silane. Moreover, it is also possible to add a high boiler and flow nature increases more. Moreover, membrane formation temperature is good below 250 degrees C, and its 100 degrees C or less are preferably good. Furthermore, the duty of the pulse for impressing RF power intermittently has 10 - 70% of desirable range.

[0042] Although the fluorine content silicon oxide is formed in the 3rd and the 4th example using the parallel monotonous type plasma CVD equipment which uses RF power with a frequency of 13.56MHz, the plasma CVD method by the electron cyclotron resonance (efficient consumer response) which uses microwave, or a photochemistry vapor growth can be used for this invention also except this.

[0043] Drawing 9 is the schematic diagram of the chemical-vapor-deposition equipment for explaining the example of further others of this invention.

[0044] It sets to this drawing and is O₂. Gas is controlled by the flow controller 906 and it introduces into an ozonator 905, and ozone is generated and it introduces into a reaction field from the dispersion head 904. Simultaneously, it is N₂. After controlling gas by the flow controller 908, introducing into the bubbler 910 maintained at fixed temperature and making TEOS evaporate, it introduces into a reaction field from the dispersion head 904. SiF₄ controlled by the flow controller 909 to the system of reaction in this invention Gas is mixed. Since this halogen gas causes the chemical reaction of $\text{SiF}_4 + 2\text{H}_2\text{O} = \text{SiO}_2 + 4\text{HF}$, the moisture content in a film made into the problem can be decreased or less [conventional] to 1/3 by adding to the system of reaction of a silicon-oxide film. Since HF generated simultaneously is compulsorily exhausted by the duct, there is no problem that a reaction returns to a system ($\text{SiF}_4 + 2\text{H}_2\text{O}$). The fluorine atom was not detected when elemental analysis of the depth direction of this new oxide film was performed. It is mixed in a reaction field and these gas is formed on the semiconductor substrate 901 on the susceptor 102 maintained at fixed temperature at the heater 903 for heating.

[0045] Drawing which applied the new oxide film formed by this business to the semiconductor device is drawing 11 and drawing 12 which are shown below. On semiconductor substrate top 1101, as shown in drawing 11 (a), after depositing a BPSG film on the thickness of 0.5 micrometers by the ordinary-pressure vapor growth, heat treatment for 30 minutes is performed in 900-degree C nitrogen gas atmosphere, and the bottom insulator layer 1102 of wiring is formed. Next, on the bottom insulator layer 1102 of wiring, the aluminum film containing copper and silicon is deposited by the thickness of 1 micrometer by the sputtering method, and carries out patterning, and wiring 1103 is formed. next, a front face including wiring 1103 -- parallel monotonous type single-wafer-processing plasma-chemistry vapor-growth equipment -- using -- the substrate temperature of 375 degrees C, a pressure 1, 0Torr, and 13.56MHz RF power 2 W/cm² On conditions, the 0.4-micrometer plasma TEOSU film 1104 is formed using TEOS and oxygen gas.

[0046] On condition that the above, as shown in drawing 11 (b) after forming the plasma TEOSU film 1104, parallel monotonous type single-wafer-processing ordinary-pressure vapor-growth equipment is used, and it is the substrate temperature of 400 degrees C, TEOS flow rate 50sccm, and SiF₄. The new oxide film 1105 with a thickness of 0.8 micrometers is deposited on condition that flow rate 50sccm and ozone flow rate 400sccm.

[0047] Furthermore, as shown in drawing 11 (c), the organic silica film 1106 is formed by the thickness of about 1 micrometer by the spin applying method on the new oxide film 1105.

[0048] Next, as shown in drawing 11 (d), an parallel monotonous type batch-type reactive ion etching system is used, and it is CF₄. Quantity-of-gas-flow 100sccm and O₂ It is 2 0.3W [cm] RF power to quantity-of-gas-flow 15sccm, pressure 0.1Torr, the frequency of 13.56MHz, and a row. On conditions, the organic silica film 1106 all reaches, etchback of a part of front face of the new oxide film 1105 is carried out, and flattening of the front face of the new oxide film 1105 is carried out. Here, the etching rate of the new oxide film 1105 is made almost the same as the etching rate of the organic silica film 1106, or it enlarges a little.

[0049] Finally, as shown in drawing 11 (e), the plasma TEOSU film 1108 is deposited by the thickness of 0.4 micrometers on the new oxide film 1107 by which flattening was carried out.

[0050] On the other hand, as shown in drawing 12 (a), after depositing a BPSG film by the ordinary-pressure vapor growth on semiconductor substrate top 1201 in drawing 12 at the thickness of 0.5 micrometers, heat treatment for 30 minutes is performed in 900-degree C nitrogen gas atmosphere, and the bottom insulator layer 1202 of wiring is formed. Next, on the bottom insulator layer 1202 of wiring, the aluminum film containing copper and silicon is deposited by the thickness of 1 micrometer by the sputtering method, and carries out patterning, and wiring 1203 is formed. Then, parallel monotonous type single-wafer-processing ordinary-pressure vapor-growth equipment is used, and it is the substrate temperature of 400 degrees C, TEOS flow rate 50sccm, and SiF₄. The new oxide film 1204 with a thickness of 0.8 micrometers is deposited on condition that flow rate 50sccm and ozone flow rate 400sccm. Furthermore, as shown in drawing 12 (b), the organic silica film 1205 is formed by the thickness of about 1 micrometer by the spin applying method on the new oxide film 1204.

[0051] Next, as shown in drawing 12 (c), an parallel monotonous type batch-type reactive ion etching system is used, and it is CF₄. Quantity-of-gas-flow 100sccm and O₂ It is 2 0.3W [cm] RF power to quantity-of-gas-flow 15sccm, pressure 0.1Torr, the frequency of 13.56MHz, and a row. On conditions, the organic silica film 1205 all reaches, etchback of a part of front face of the

new oxide film 1204 is carried out, and flattening of the front face of the new oxide film 1204 is carried out. Here, the etching rate of the new oxide film 1204 is made almost the same as the etching rate of the organic silica film 1205, or it enlarges a little.

[0052] Finally, as shown in drawing 12 (d), the plasma TEOSU film 1207 is deposited by the thickness of 0.4 micrometers on the new oxide film 1206 by which flattening was carried out.

[0053] Drawing 10 is the schematic diagram of the chemical-vapor-deposition equipment for explaining the example of further others of this invention.

[0054] It sets to this drawing and is O₂. Gas is controlled by the flow controller 1006 and it introduces into the ozone nascent state 1005, and ozone is generated and it introduces into a reaction field from the dispersion head 1004. Simultaneously, it is N₂. After controlling gas by the flow controller 1008, introducing into 1010 the bubbler maintained at fixed temperature and making TEOS evaporate, it introduces into a reaction field from the dispersion head 1004. N₂ controlled by the flow controller 1009 when introducing TEOS into a reaction field here Gas is introduced into the bubbler 1011 maintained at fixed temperature, and TEFS is added. By the pulse-like addition bulb 212, this TEFS is introduced into a reaction field from the dispersion head 1004 at intervals of 10 seconds. By this TEFS pulse-like addition, the rate in the silicon-oxide film of the fluorine atom contained by the conventional chemical-vapor-deposition method decreases to 1/2 over the past. Thereby, suppression of the increase in a leakage current and an etching rate made into a problem by content of the fluorine atom which is a different atom is attained conventionally, with level difference covering nature maintained.

[0055] Even if it uses the chemical-vapor-deposition equipment of drawing 10, it cannot be overemphasized that drawing 11 and two kinds of semiconductor devices of drawing 12 which were stated in the example 5 can be manufactured similarly.

[0056]

[Effect of the Invention] As explained above, the formation of the layer insulation film which whose flow nature was high, namely, was excellent in the embedded nature between detailed wiring spaces by the chemical-vapor-deposition method using the fluoro alkoxysilane and the oxidizing gas which have a three or more-carbon number alkyl group of this invention is attained.

Furthermore, in the chemical-vapor-deposition method using the fluoro alkoxysilane and the oxidizing gas which have an one or more-carbon number alkyl group, when the boiling point makes a high boiler 90 degrees C or more add, making the same flow nature give is festering, and the formation of a layer insulation film excellent in the embedded nature between wiring spaces of this invention is attained. Moreover, as for the remains moisture content of the formed fluorine content silicon oxide, sufficiently few, the amount of moisture absorption also becomes 1/4 or less [conventional], and degradation of a device property has the effect of being pressed down to 2% or less. In the chemical-vapor-deposition method using the fluoro alkoxysilane and the oxidizing gas of this invention, even if it makes at least one of alkoxysilane, such as a tetraethyl orthochromatic silicate, alkyl alkoxysilane, an organic siloxane, and organic silanes add, the same effect is acquired further again.

[0057] Therefore, this invention is useful to the flattening layer insulation film formation for the multilayer interconnections of a VLSI device.

[0058] Furthermore, since this invention is the method of this insulator layer adding a halogenation inorganic substance in an organic silane ozone system, exhausting subgeneration gas HF compulsorily by the duct, and forming a silicon-oxide film in the chemical-vapor-deposition method an insulator layer is formed on a front face including wiring, the moisture in a film can be decreased to the state completely near zero, without including a fluorine atom at all. Moreover, since another invention is the chemical-vapor-deposition method which forms the silicon-oxide film which added the organic silane containing a halogen in the shape of a pulse, the rate of a fluorine atom decreases compared with the conventional technology.

[0059] Therefore, with the good level difference covering nature of a TEOS film and a TEFS film maintained, there is no generating of a void and the moisture and fluorine atom in a silicon-oxide film can suppress the problem of the membranous reliability fall of making a leakage current and an etching rate increase.

[Translation done.]